5   the at least one of the pipeline stages including processing circuitry with an

6   active state which is entered when the data received by the at least one of the

7   pipeline stages has a predetermined activation pattern, the predetermined activation

8   pattern corresponding to one of the different standards;

9   the at least one of the pipeline stages including a state machine having a

10   current state and a previous state; and

11   wherein the at least one of the pipeline stages is activated upon recognition of

12   the predetermined activation pattern only upon a predetermined transition from the

13   previous state to the current state.

1   2.   The pipeline system of claim 1, wherein the processing circuitry has an

2   inactive state, in which the at least one of the pipeline stages passes data to a

3   following pipeline stage without processing.

1   3.   The pipeline system of claim 1, wherein the sequence of pipeline

2   stages includes at least one spatial decoder stage.

1   4.   The pipeline system of claim 1, wherein the sequence of pipeline

2   stages includes at least one temporal decoder stage.

1   5.The pipeline system of claim 1, wherein the at least one of the pipeline

2   stages is a spatial decoder stage.

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